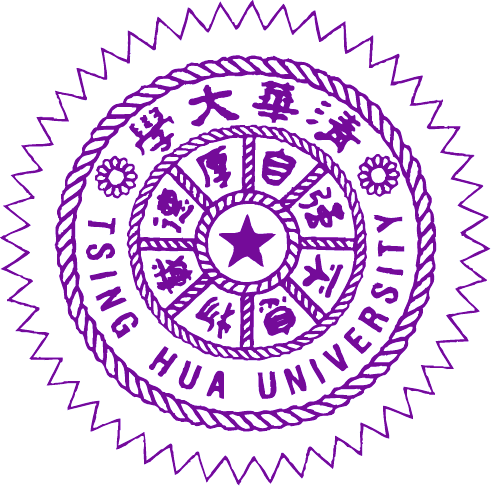
Analog IC Design Homework 3

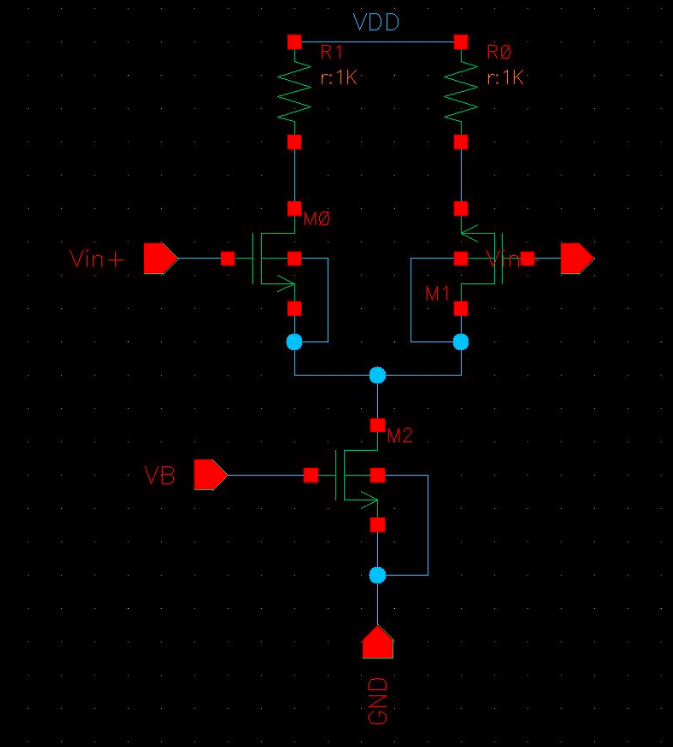


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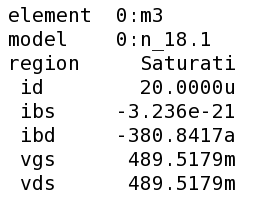
1.

Schematic:



(a) To find a proper to let the drain current of =20uA, I connect with a 20uA current source, and =.

from .lis file:

 = is about 489.5mV, I choose 0.49

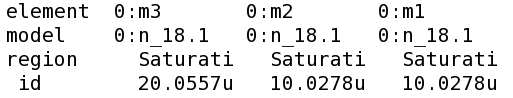
|| = \*(//), so if we want to raise the gain, we expect (1) to be larger, which means larger W

(2) to be larger, which means larger L, but //, so the impact of L is narrowed. Thus, W is my trial priority.

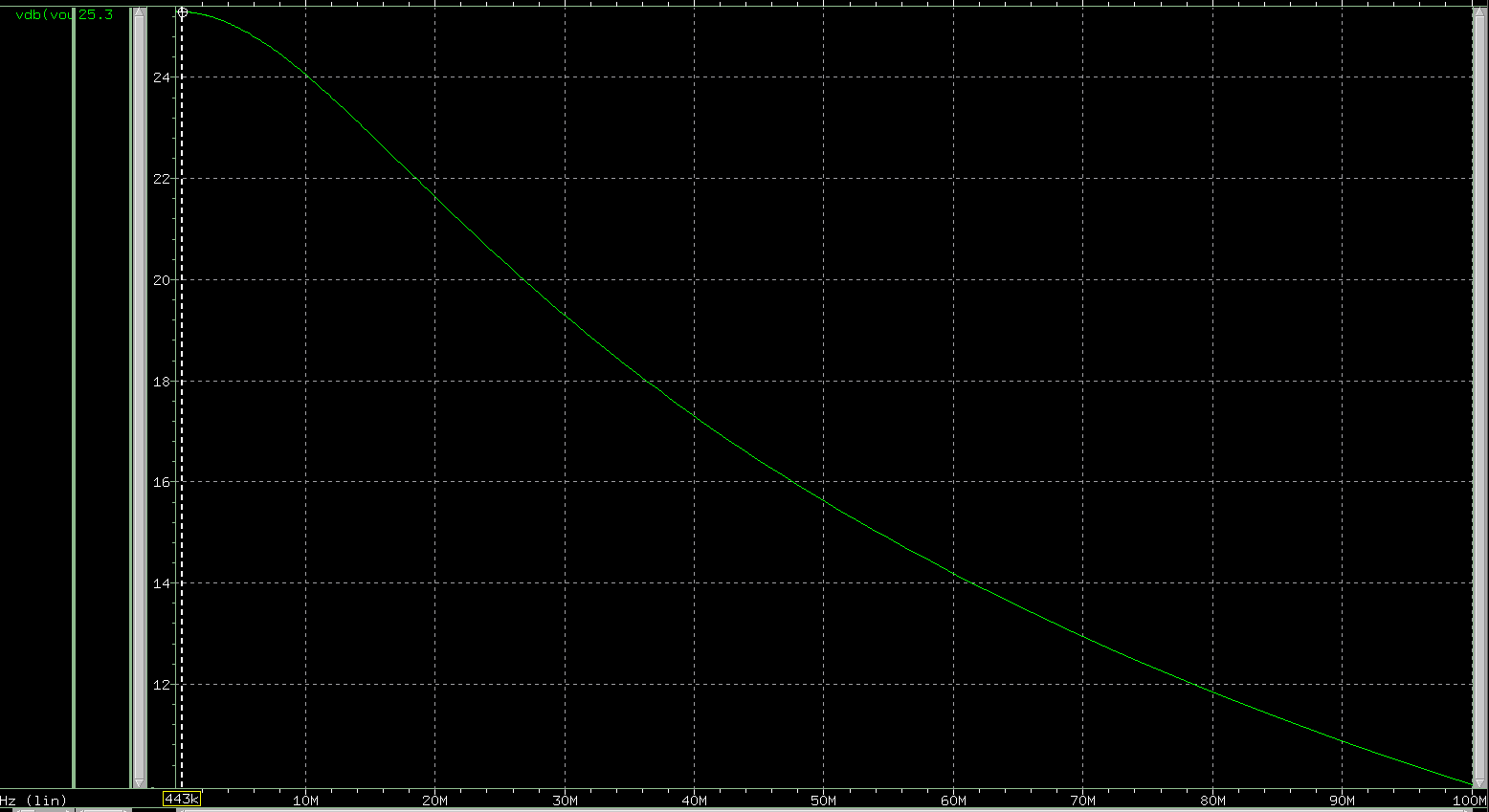
(3) to be larger, which = 100k.

And my design is = = 84u /2.8u.

from .lis file:



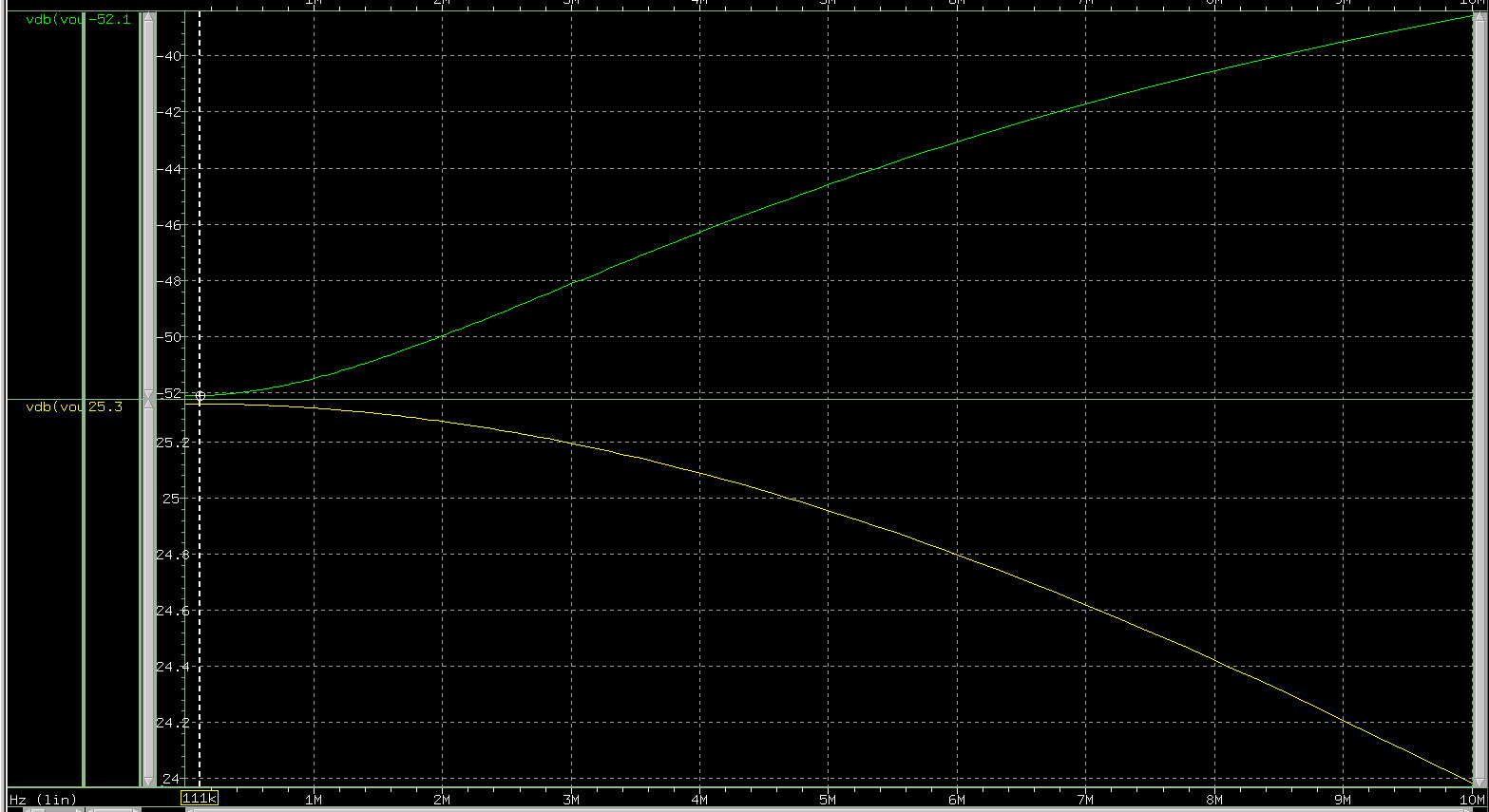
The voltage gain= 25.3dB > 20dB:



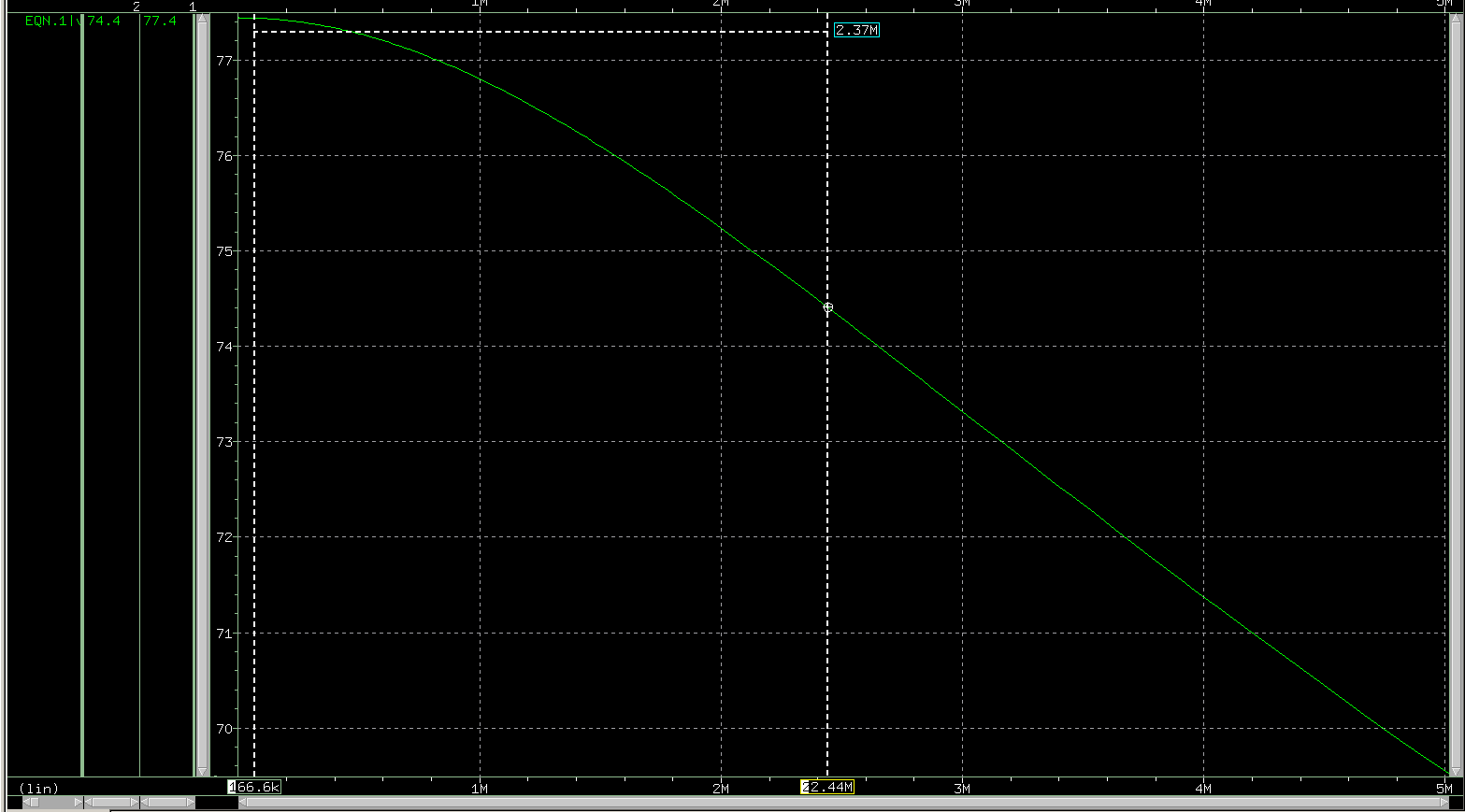
(b) becomes 92.4u/2u.

(i) Without :

|| = 25.3dB, || = 52.1dB



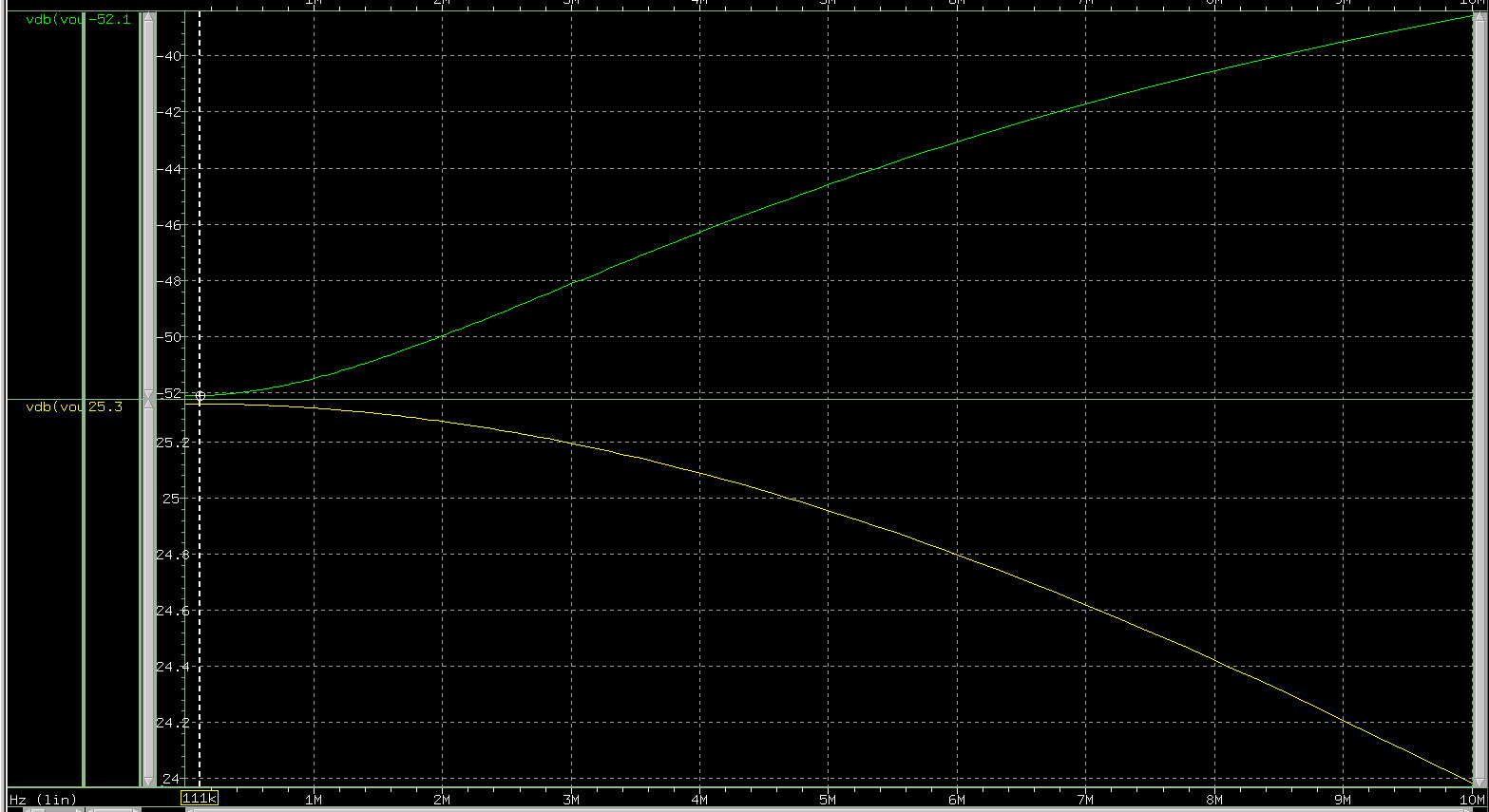
At low freq. CMRR = | / | = 25.3dB - (-52.1dB) = 77.4dB



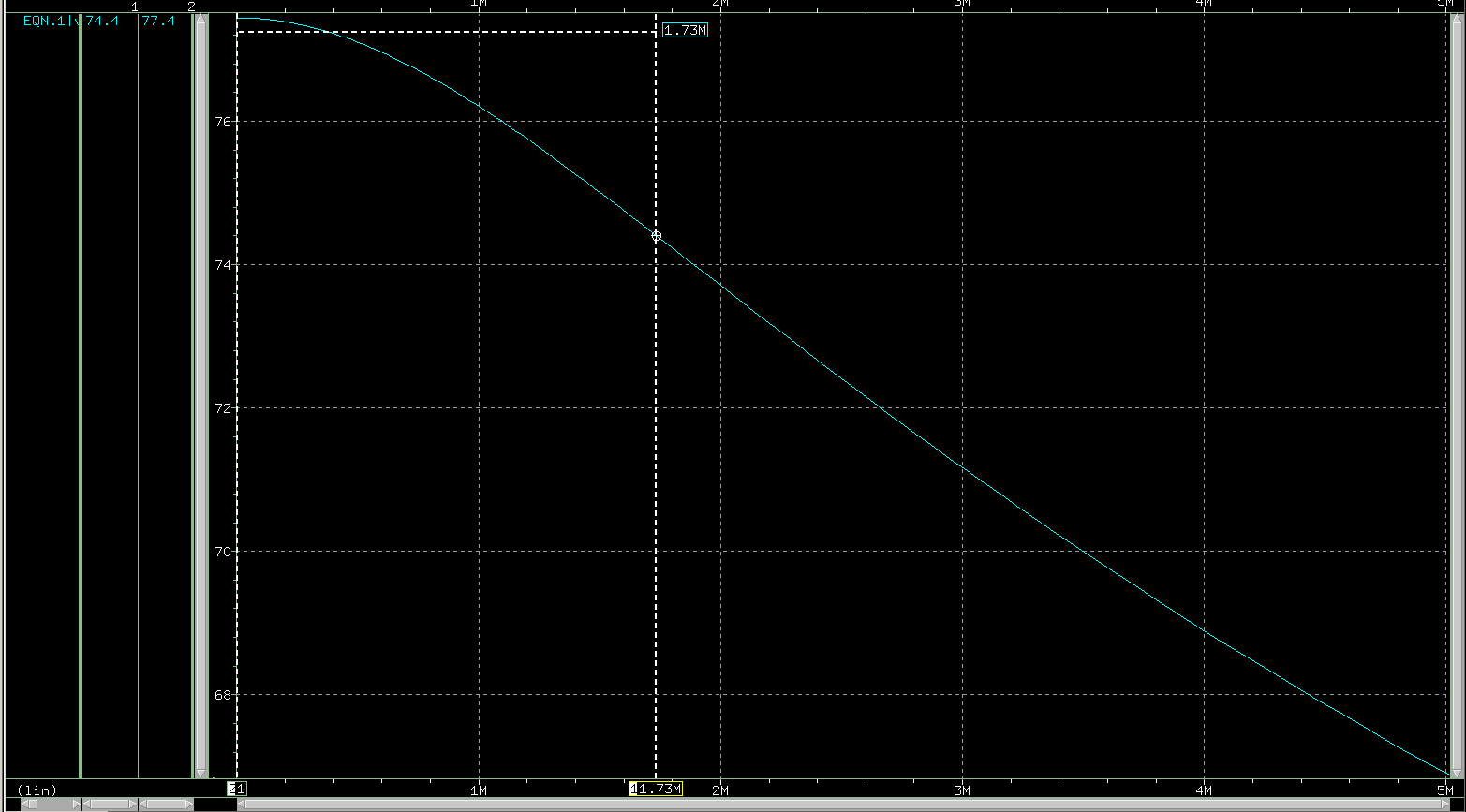
from the figure, -3dB bandwidth without = 2.44M.

(ii) With from P to ground:

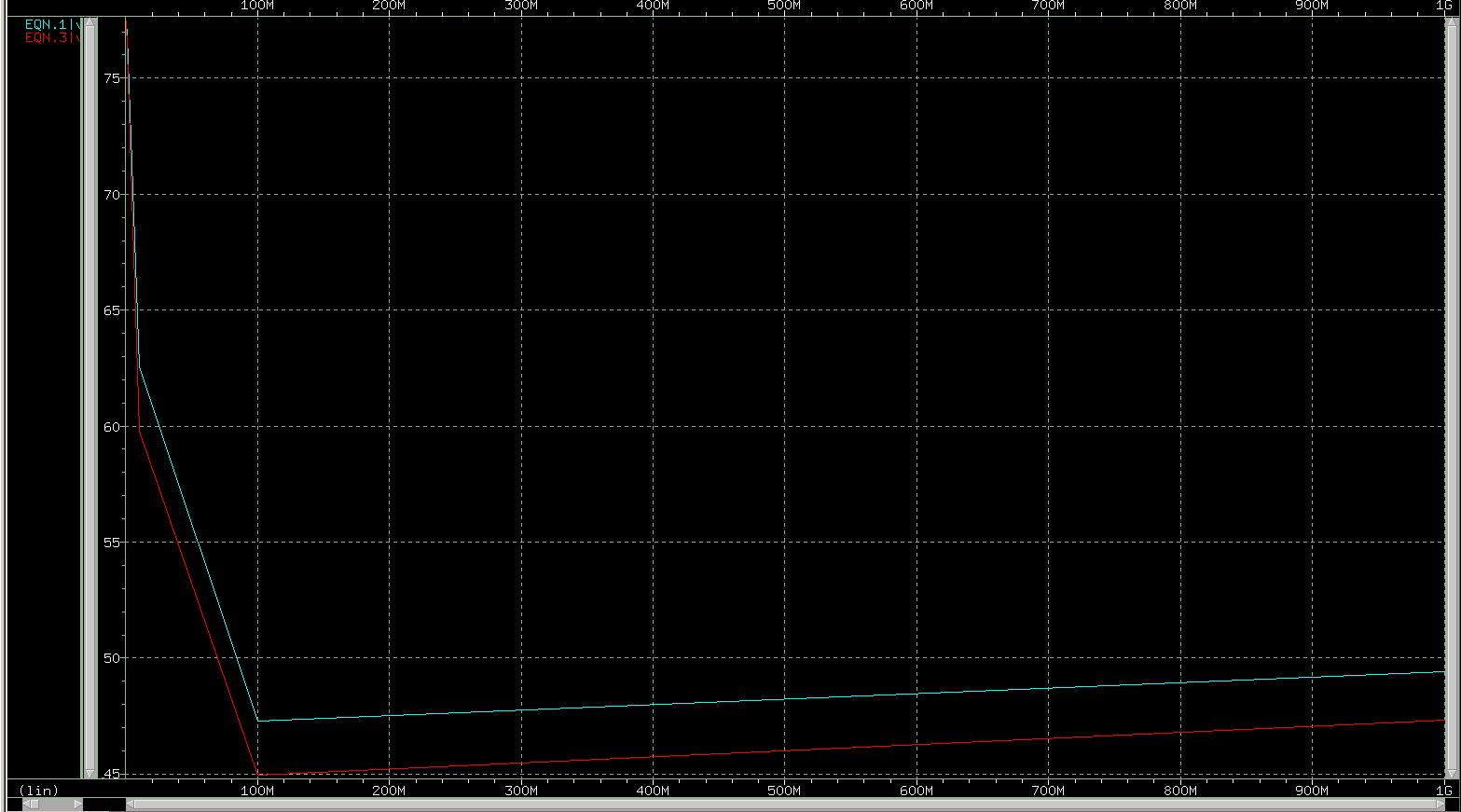
|| = 25.3dB, || = 52.1dB



At low freq. CMRR = | / | = 25.3dB - (-52.1dB) = 77.4dB is same as that without .



from the figure, -3dB bandwidth with = 1.73M.



Red curve: CMRR with ; Blue curve: CMRR without

(iii) Comment:

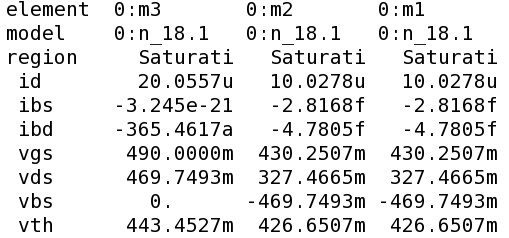
The common-mode to differential conversion becomes significant at high frequencies, since is shunted by .

= and at high frequencies, Z() = 1/jw becomes smaller, so // becomes smaller, and becomes larger, resulting in smaller CMRR.

I compare the -3dB bandwidth , and the one without is bigger than the one with . It's reasonable since CMRR with decrease faster, resulting in smaller bandwidth.

(c)

To calculate for all MOS saturation:

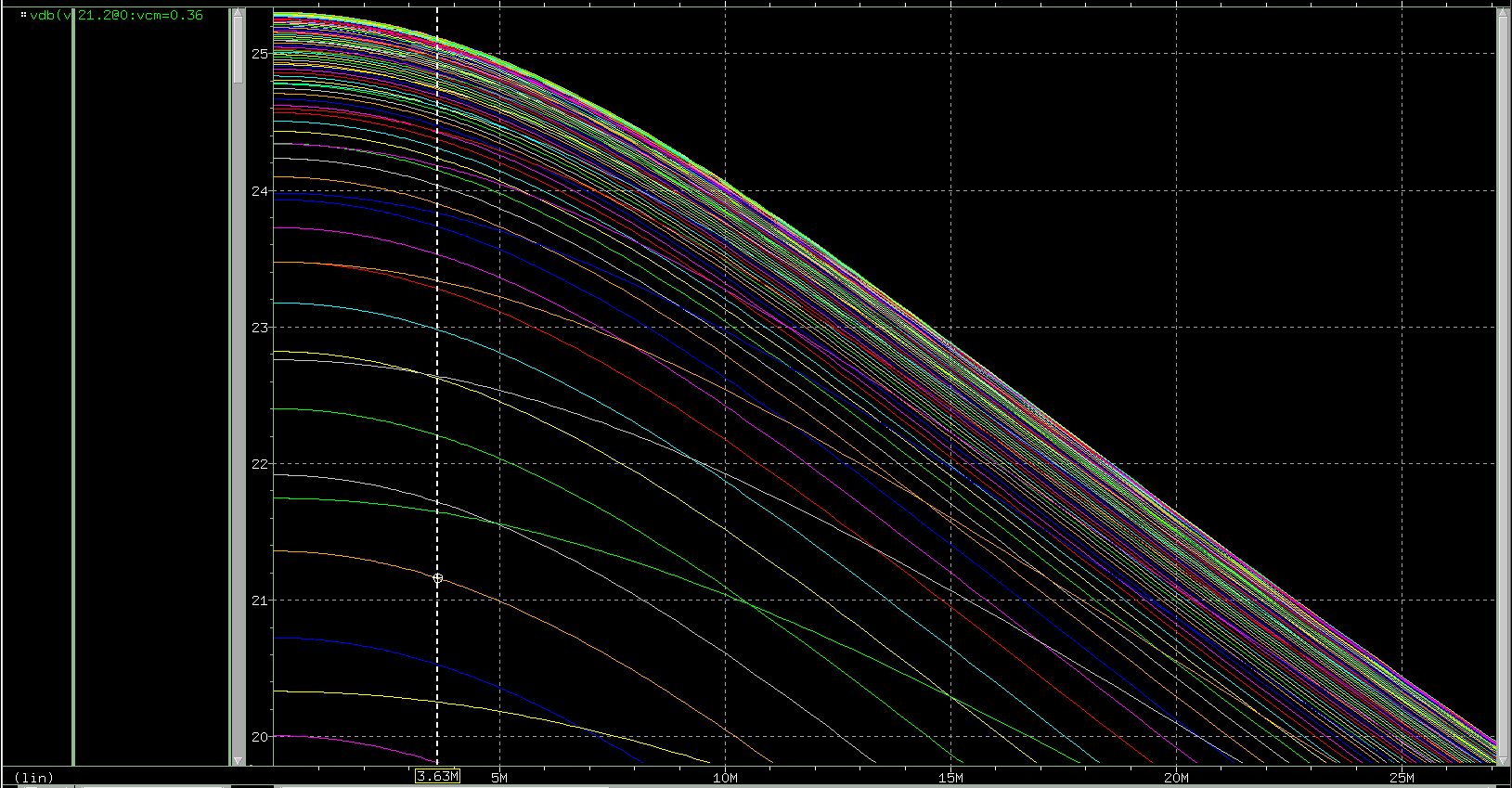
from .lis file

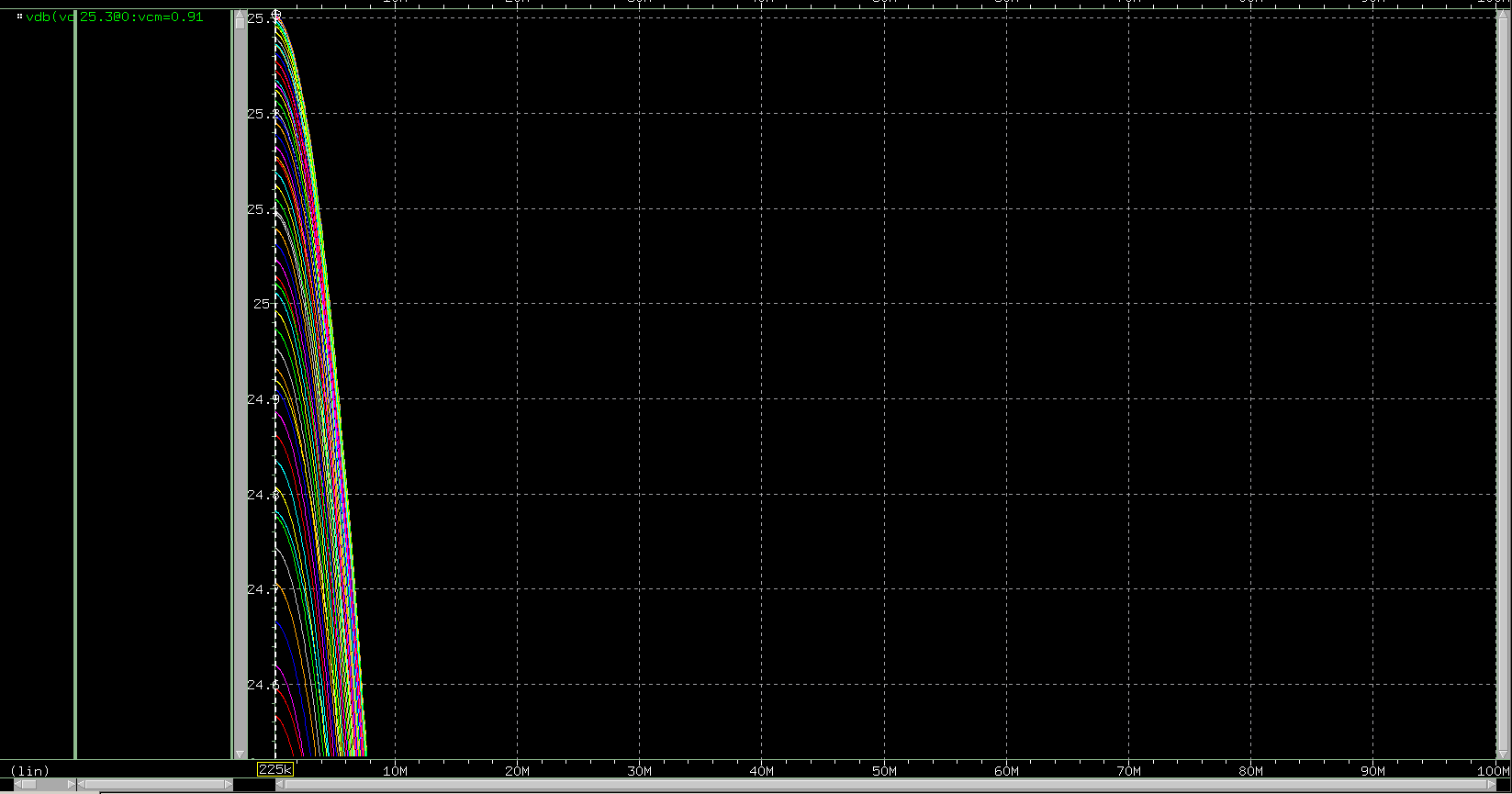


-> 0.43025+(0.49-0.44345)≦≦1.8-100k\*+0.42665

-> 0.4768≦≦1.22665

And from simulation, 0.36≦≦0.91



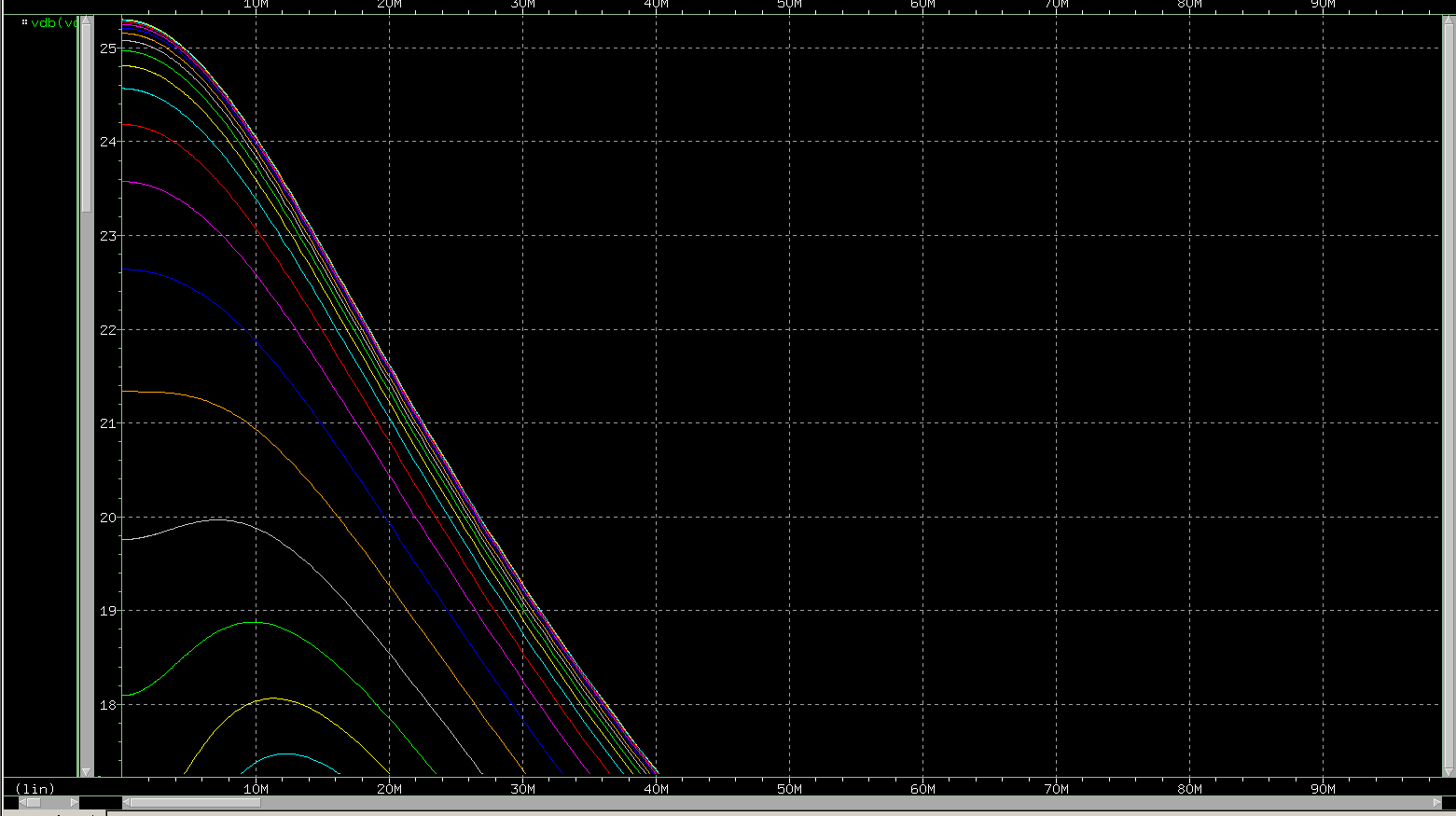


So combine above results, our desire IMCR is 0.4768≦≦0.91

(d)

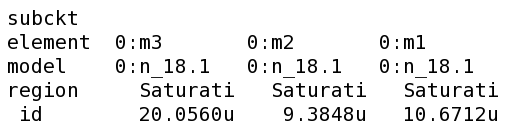
The maximum differential input that the circuit can handle:

Δ = = () = (0.43-0.426) =0.00565V

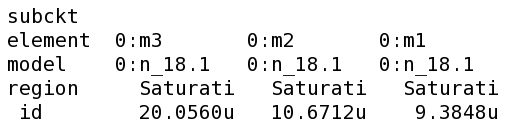


Above figure is the simulation, and find the one with all MOS in saturation from .lis file(shown below),

diff8965.png



diff9035.png



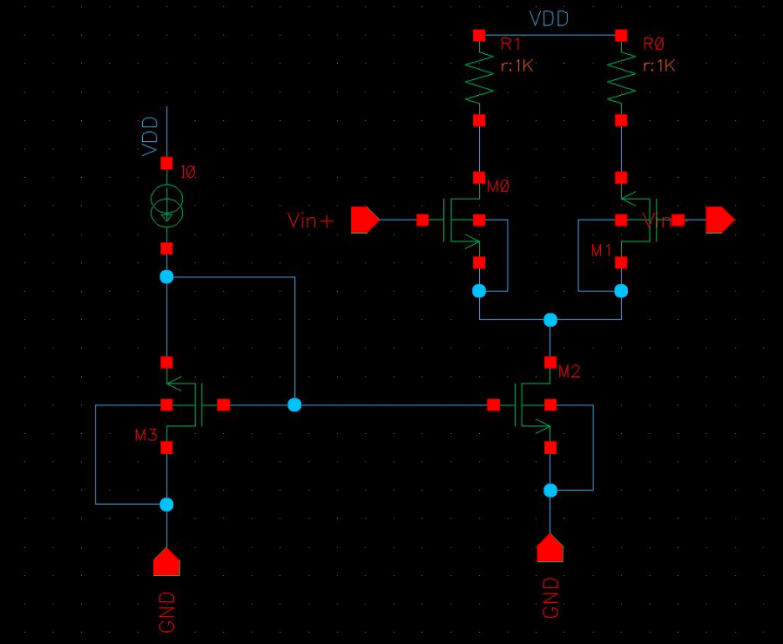
So the input differential maximum is 0.9035-0.8965=0.007V

and the input differential range Δis from 0 to 0.0035.

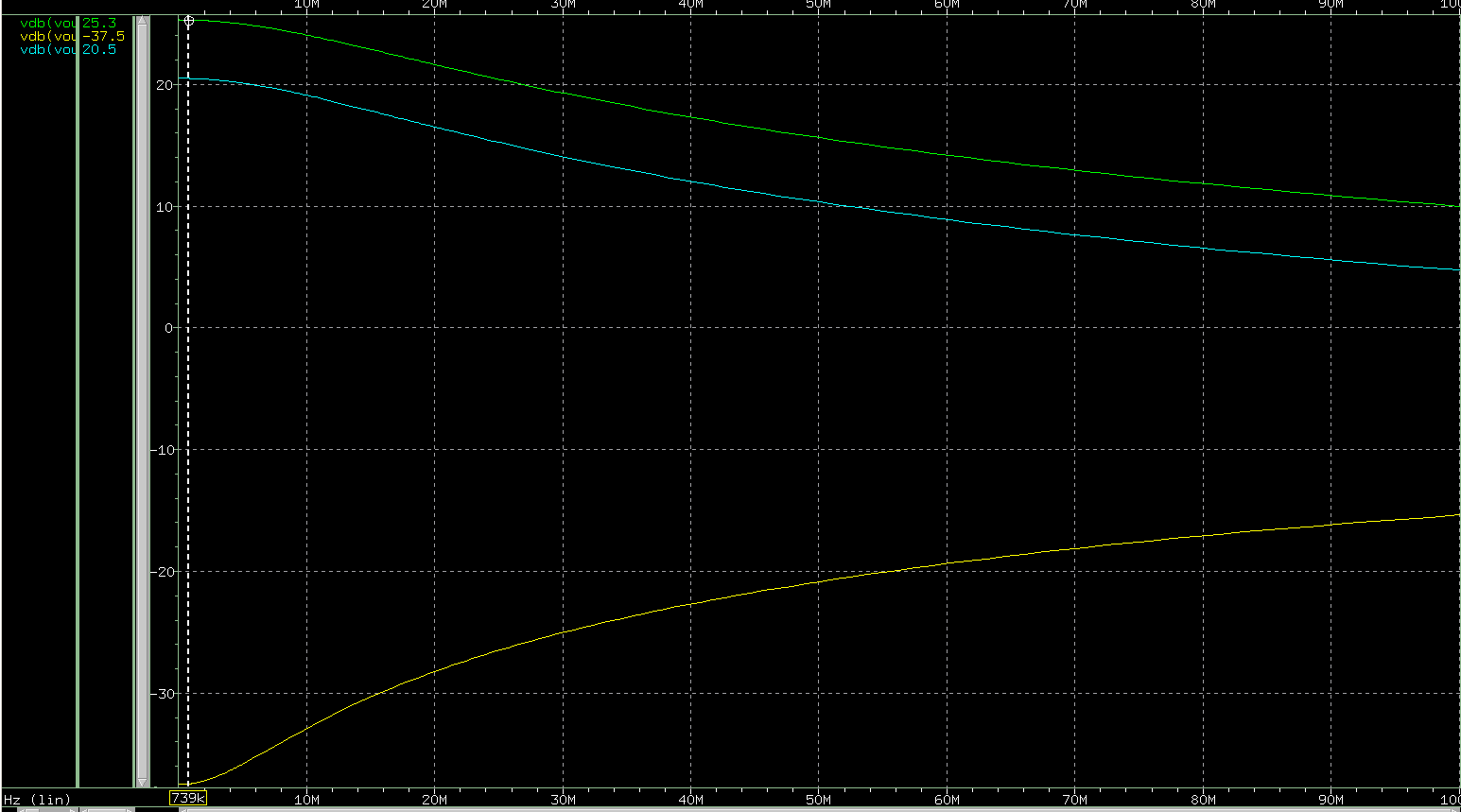
It's reasonable that it's smaller than calculation, since we want all MOS to be saturation.

(e)

Schematic:

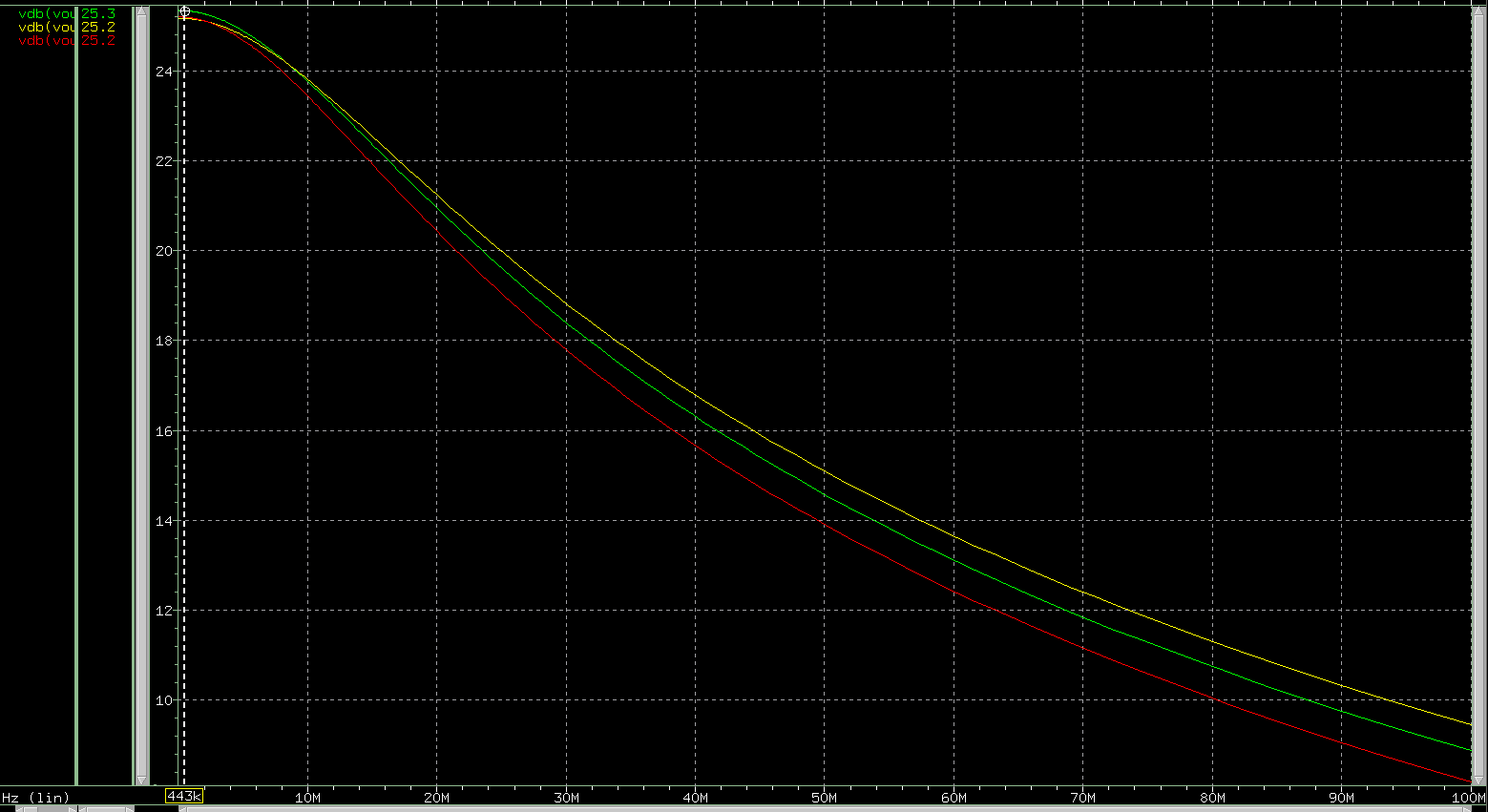


The gain of using ideal voltage source to generate :



Green curve: TT Yellow curve: FF Blue curve: SS

The gain of using current mirror to generate :



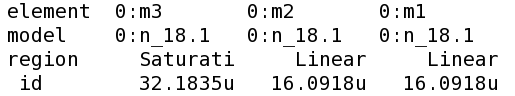
Green curve: TT Yellow curve: FF Red curve: SS

Comment:

(i) For TT corner, both methods generating bias voltage will have all MOS in saturation, and reach a voltage gain of 25.3.

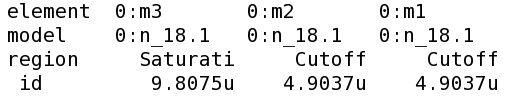
(ii) For FF corner, when using current mirror, we can still get a voltage gain of 25.2 and all MOS in saturation at the same time.

But when using ideal voltage source, the gain || can reach 37.5, but not all MOS in saturation.

 from .lis file

(iii) For SS corner, when using current mirror, we can still get a voltage gain of 25.2 and all MOS in saturation at the same time.

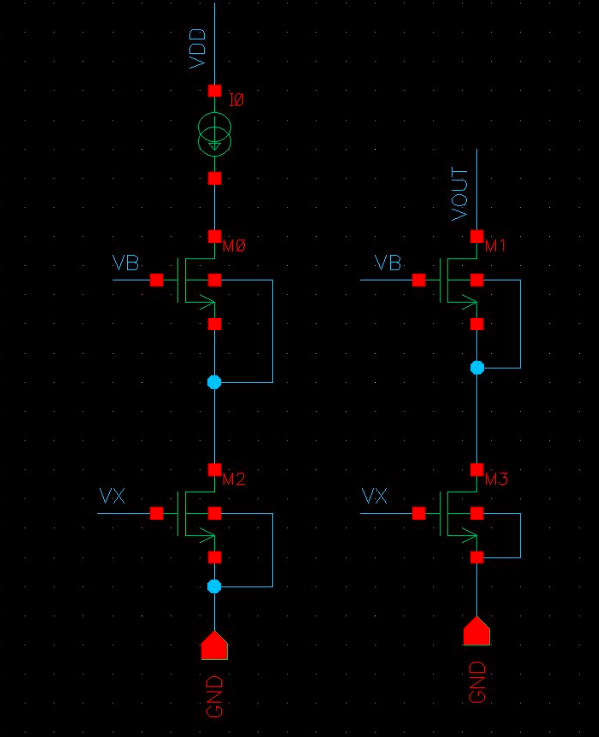
But when using ideal voltage source, the gain will drop to 20.5 and not all MOS in saturation.

 from .lis file

(iv) We can observe that using current mirror to generate bias voltage is better in all three TT, FF, SS corners, since when operating in different corners, the parameters changed, so if we use the same ideal voltage source, it might not operate in saturation.

2.

Schematic:

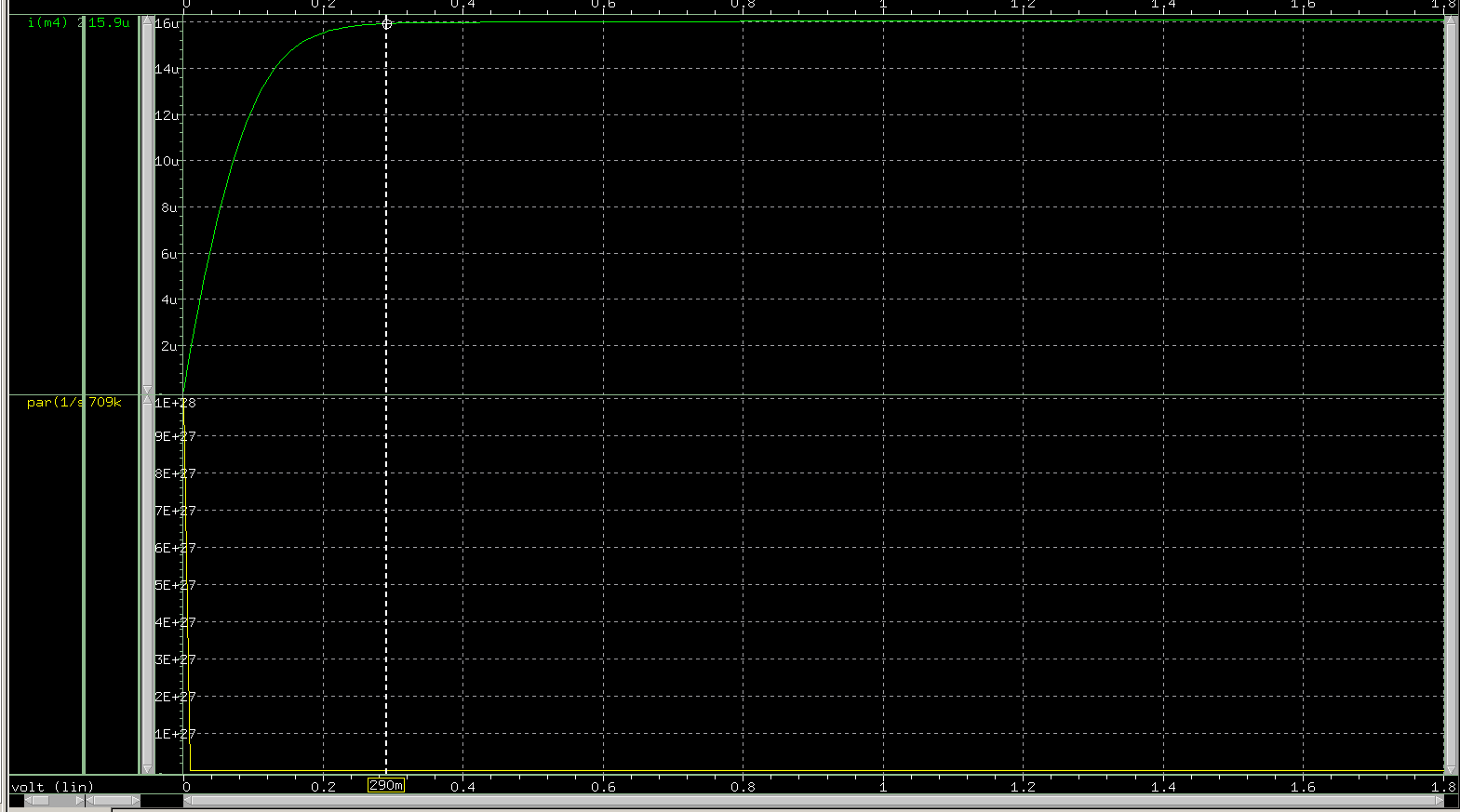


(a)

We want to be 16uA and is 4uA, so we want

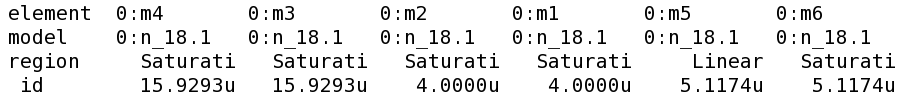
= . I use the same length for all of the transistors so as to minimize errors due to the side diffusion of the source and drain areas, and make the multiple finger of 4.

For M1, M2 in saturation, +() ≦ ≦



(b)

M6 is guaranteed to be in saturation, since it's gate and drain are connected. But with all transistors in saturation region, M5 can only be in linear region, because = = + , > and thus - > .



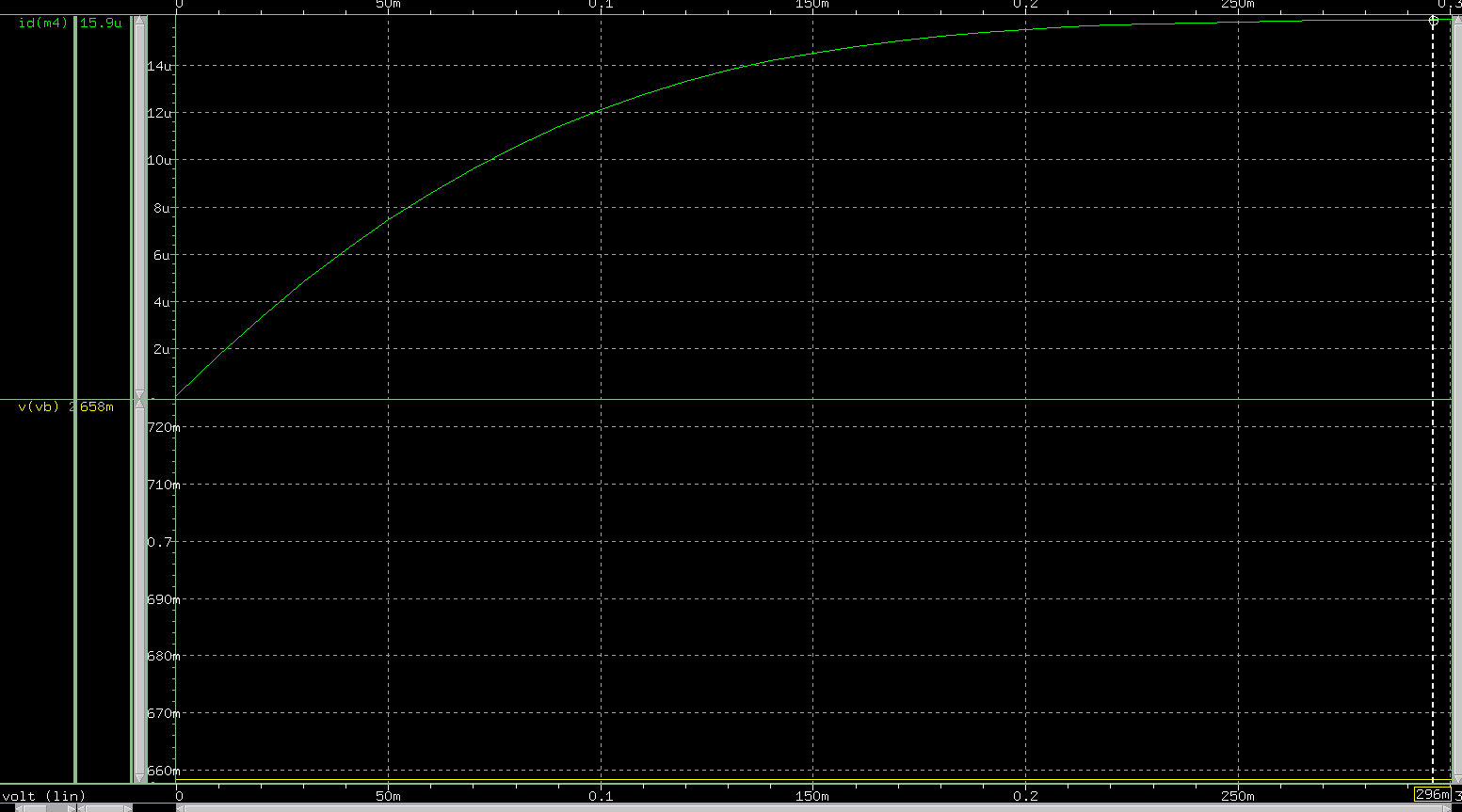
So we can calculate the current:

For M6: = 2

For M5: = (2()-2)

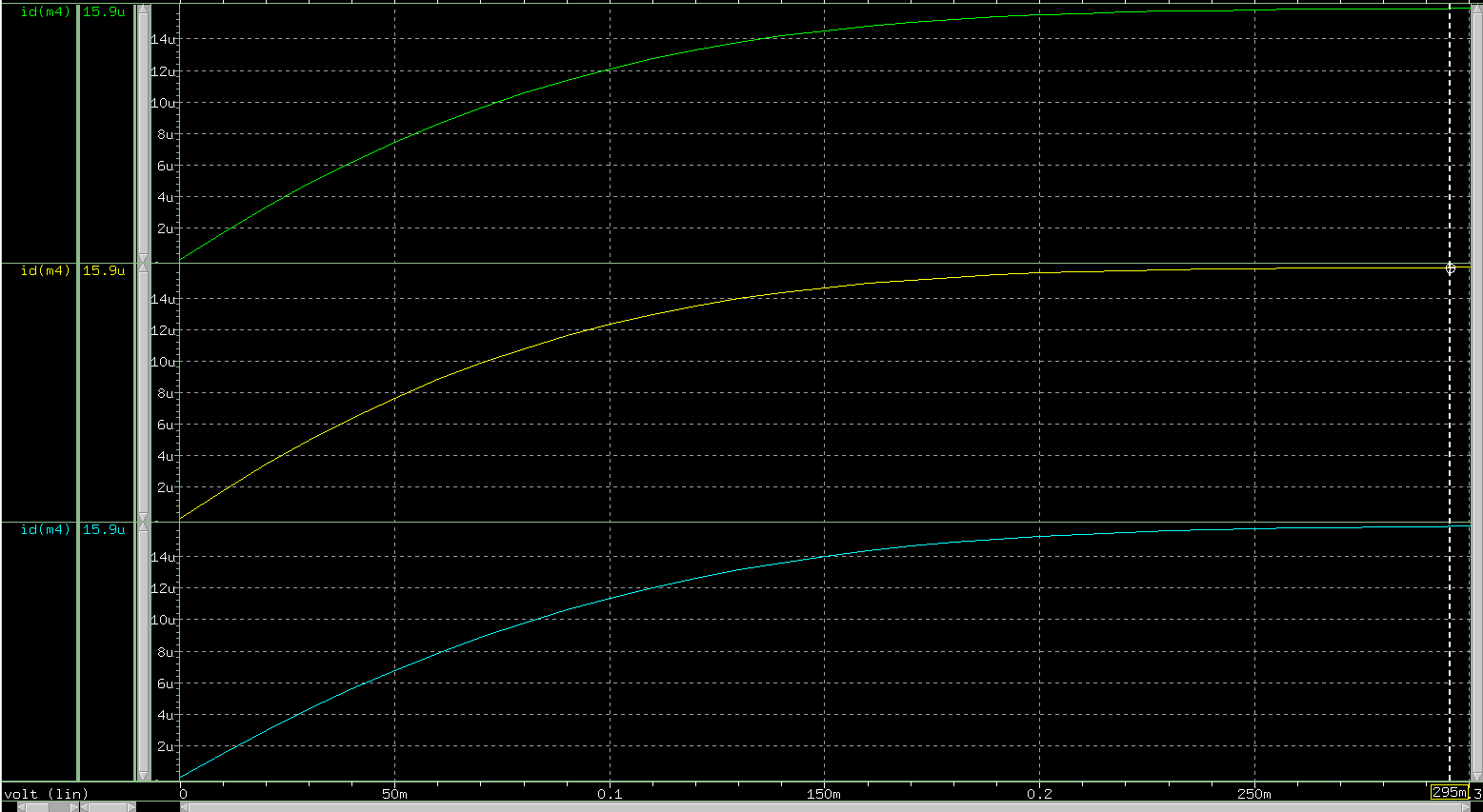
After calculation, we found that is equal to times 3, so I design = 2u/4.5u and = 2u/1.5u.

And can reach 16u, same as the result of giving bias voltage. And there is about 40mV difference from the original one, but I reckon that a roughly 5% difference is acceptable.



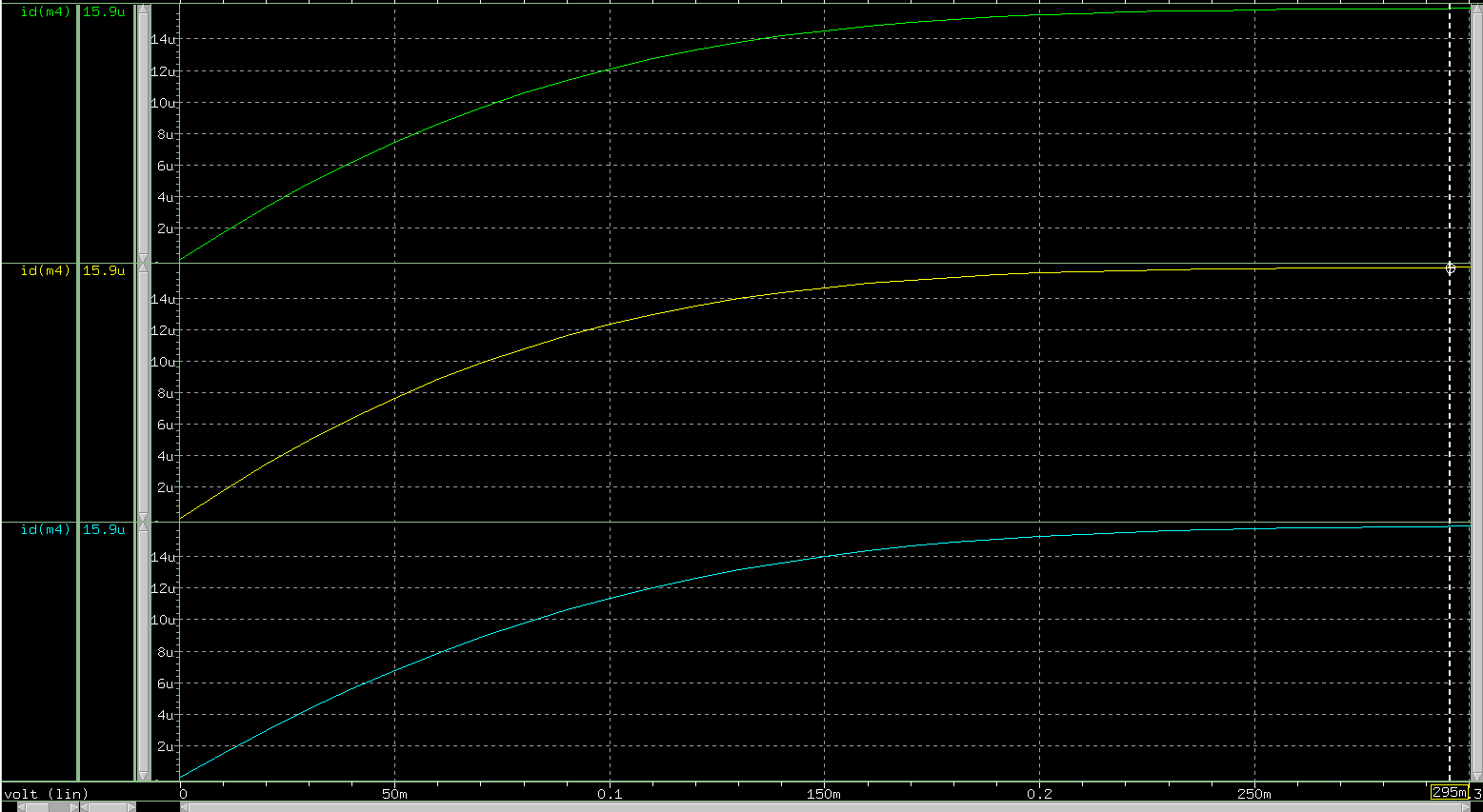
(c)

Figure of output current when using bias generation circuit:



Green curve: TT Yellow curve: FF Blue curve: SS

Figure of output current when using ideal voltage source:



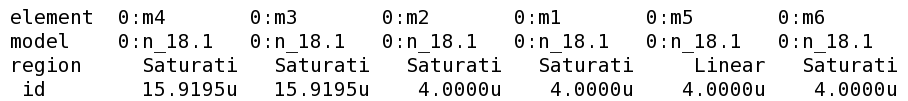
Green curve: TT Yellow curve: FF Blue curve: SS

Comment:

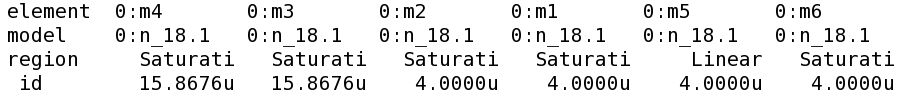
(i) Using bias generation circuit, we have close to 16uA, and from .lis file, we found only M5 in linear region as expected.

(ii) Using ideal voltage source, we have close to 16uA as well, we concern that there might be transistor other than M5 not being in saturation. But in this case, from .lis file(shown below), we found it alright.

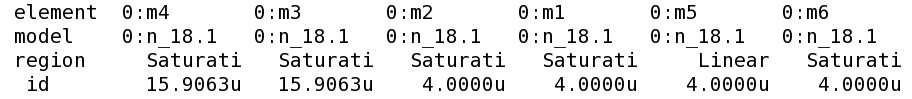
TT:



FF:

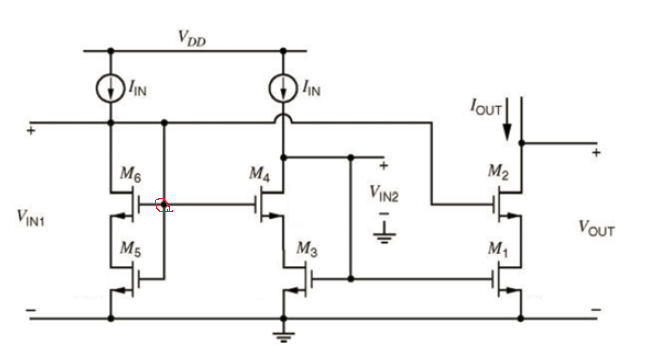


SS:



(d) M6 is guaranteed to be in saturation, since it's gate and drain are connected. But with all transistors in saturation region, M5 can only be in linear region, because = = + , > and thus - > .

(e)



= the voltage with red circle in the figure above = (M3)+()(M4) = 2+